RAKE RECEPTION APPARATUS

[0001]

FIELD OF THE INVENTION

This invention relates to a reception apparatus for a spread spectrum communication system. More particularly, it relates to a reception apparatus that may be used with advantage in particular in a cellular telephone system of the CDMA system.

[0002]

BACKGROUND OF THE INVENTION

In the spread spectrum communication system, a carrier wave is modulated by transmission data and, in addition, the carrier wave is multiplied with the pseudorandom noise (PN) code, on the transmitting side, so that the carrier wave is transmitted as it is modulated with the PN code and as the frequency spectrum is spread. On the receiving side, the carrier wave is multiplied with the same PN code as that used on the transmitting side. If the PN code is the same PN code as and in phase with that used in transmission, despreading occurs to produce a modulated output, which is demodulated to derive reception data. In the spread spectrum communication system, as discussed above, the received signal is despread, so that the PN sequence which is the same as that used on the transmitting side not only in pattern but also in phase is needed. The code division multiple access (CDMA) system enables multiple connection by changing the pattern and the phase and is recently finding application in mobile communication in that it is superior in interference combatting

and intercept combatting performance and also in that it is able to realize reception characteristics that are optimal in a multi-path environment.

[0003]

In the CDMA-based mobile communication system, there is used a path diversity system (RAKE system) in which plural path signals are separately despread and demodulated by plural receivers and plural path signals are separately despread and demodulated by plural receivers, in order to reduce the effect of fading by the multipath propagation route and also in order to improve the signal-to-noise ratio.

[0004]

As means for establishing and holding synchronization and demodulation under complex multipath propagation conditions, such a configuration is routinely used in which delay characteristics are found from path to path by a searcher, an initial phase is set for a plurality of finger circuits and outputs of the respective finger circuits are synthesized by a synthesis circuit depending on the reception signal intensity (RSSI) and on the signal to noise ratio (S/N ratio).

[0005]

In order to maintain synchronization (tracking) after establishment of synchronization by the initial phase, such a configuration is widely used in which a delay lock loop (DLL) is provided for each finger circuit to follow the jitter from path to path.

[0006]

In a well-known manner, this DLL circuit typically includes a PN sequence generator for generating a PN sequence and two multipliers for

detecting the correlation with respect to the reception signal by signals leading and lagging an optimum phase a preset chip (or stage of elements). Outputs of these two multipliers are passed through filters and detected by a detector and a difference is taken of respective detector outputs (correlated outputs), this difference crossing the zero at an optimum tracking point for which the code phase is optimal. The oscillation frequency of a voltage controlled oscillator is controlled by a control signal obtained on smoothing the difference of the correlated values through a loop filter, with an output clock of the voltage controlled oscillator being fed to the PN sequence generator. Such a PN sequence with the optimal code phase (reference signal) is taken out from the DLL circuit for despreading and demodulation in the finger circuit.

[0007]

SUMMARY OF THE DISCLOSURE

Meanwhile, there are contained in the phase jitter of the multipath reception signal those components produced due to e.g., movement of the terminal itself and which are changed in a concerted fashion between plural paths.

[0008]

Moreover, in the mobile communication system, recently proposed, there is used such a system which controls the transmission timing on the terminal side. In such system, it may be an occurrence that phase jitter components changing in unison in the respective paths as seen from the reception side are predominant.

[0009]

For coping with such multipath phase jitter, a DLL circuit needs to be provided from one finger circuit to another. Moreover, the phase control of the respective DLL circuits need to be performed in unison, as a result of which the circuit scale and the power consumption of the reception device are increased.

[0010]

For example, in the JP Patent Kokai JP-A-10-209918, there is disclosed a structure of a reception device in which plural finger circuits are provided with DLLs for synchronization tracking, each DLL having a loop filter, thus increasing the circuit scale. In order to resolve the problem of increasing the communication scale, each finger circuit includes a DLL for synchronization tracking with the plural finger circuits co-owning a loop filter (complete integration type order-two loop filter) forming a portion of the DLL.

[0011]

There is much to be desired in the art as aforementioned.

It is therefore an object of the present invention to overcome the above problem and provide a device which, while maintaining the function for tracking the phase jitter of the multipath propagation route, is able to reduce the circuit scale to lower the power consumption.

[0012]

According to a first aspect of the present invention, there is provided a RAKE reception apparatus having a delay lock loop circuit, termed "DLL circuit", herein, for performing control to keep synchronization for a plurality of finger circuits adapted for separately

despreading and demodulating reception signals passed through respective paths of the multiple paths, the apparatus comprising:

means for selecting one of the finger circuits which is to be an object of synchronous tracking in the DLL circuit based on the information at the time of output synthesis in a RAKE combiner adapted for combining outputs of the plural circuits with output demodulated signals; and

means for aligning the phase of the DLL circuit with the phase of the selected one finger circuit.

According to a second aspect of the present invention, there is provided a RAKE reception apparatus comprising a plurality of finger circuits for receiving signals spectrum-spread by spread codes, despreading respective reception signals retrieved by a searcher adapted for retrieving respective paths from multi-path reception signals for demodulating the signals, and a RAKE combiner for combining outputs of the plural finger circuits. Each of the plural finger circuits is provided with one DLL circuit without being provided with an inner DLL circuit. The finger circuits to be tracked by the DLL circuit are switched by a changeover circuit. There is provided a control circuit for controlling the changeover circuit based on the weighting information for each finger circuit as found by the RAKE combiner for sequentially selecting the finger circuits to be tracked by the DLL circuit.

Further aspects and features of the present inventions are disclosed in the appended claims which are incorporated herein by reference thereto.

BRIEF DESCRIPTION OF THE INVENTION

Fig.1 shows a structure of an embodiment of the present invention.

Fig.2 shows a structure of a Dll circuit embodying the present invention.

Fig.3 shows a structure of the DLL circuit embodying the present invention.

Fig.4 shows the structure of a modification of the present invention.

Fig.5 shows the structure of the DLL circuit in the modification shown in Fig.4.

Fig.6 shows the structure of the finger circuit in the modification shown in Fig.3.

[0013]

PREFERRED EMBODIMENTS OF THE INVENTION

A preferred embodiment of the present invention is hereinafter explained. In the preferred embodiment of the present invention, a common one display lock loop (DLL) circuit is provided for plural finger circuits in a RAKE receiver, without providing a delay lock loop circuit (DLL circuit) for synchronization holding control for each finger circuit. The DLL circuit is caused by a changeover circuit to track an optimal finger circuit. The remaining finger circuits are adapted for being controlled by clock outputs from the DLL circuit.

[0014]

In more detail, the control circuit 3 controls the changeover circuit 4, based on the finger-based information, such as weighting information as found in synthesising demodulated output signals of the respective

finger circuits to select sequentially the finger circuits to be tracked by the DLL circuit 5.

[0015]

The clocks CK controlled by the DLL circuit 5 are fed to a PN sequence generator (13 in Fig.3) of each finger circuit to execute a synchronization keeping operation.

[0016]

In the present invention, an output signal of one finger circuit, selected by the changeover circuit 4, is received by the DLL circuit 5. Based on this signal, the DLL circuit 5 aligns the phase of the PN code, used for despreading, with the phase of the PN sequence generator in the selected one PN sequence generator.

[0017]

More specifically, the value of the shift register constituting the PN sequence generator of the selected one finger circuit is received through the changeover circuit 4 by the DLL circuit 5, and the value of the shift register constituting the PN sequence generator 60 in the DLL circuit 5 is set so as to be equal to the value of the shift register, so input, for aligning the phase of the PN sequence generator in the DLL circuit 5 with the phase of the PN sequence generator in the selected one finger circuit.

[0018]

In an alternative embodiment of the present invention, shown in Fig.4, the PN code sequence output from the PN sequence generator of the selected one finger circuit is received by the DLL circuit 5' via the changeover circuit 4, and the DLL circuit 5' then uses the PN code string

output from the PN sequence generator of the selected finger circuit for despreading such as to effect phase aligning with respect to the phase of the PN sequence generator in the finger circuit selected by the changeover circuit 4.

[0019]

In the embodiment of the present invention, as discussed above, it is possible to reduce the circuit scale of the RAKE receiver as the function of tracking the phase jitter of the multipath propagation path is maintained.

[0020]

In a preferred embodiment of the present invention, the DLL circuit includes a PN sequence generator 60 for branching reception in-phase (I)/ quadrature data (Q) input from th finger circuit, for generating and outputting early PN codes (an in-phase component PNEI and a quadrature component PNEQ) earlier in frequency divider timing than the PN codes used in the finger circuit (an in-phase component PNI and a quadrature component PNQ) and for generating and outputting late PN codes (an in-phase component PNLI and a quadrature component PNLQ) later in frequency divider timing than the PN codes used in the finger circuit (PNI and PNQ);

a first complex multiplier 51 for multiplying the I/Q data with the PN codes (an in-phase component PNEI and a quadrature component PNEQ) generated by the PN sequence generator;

a second complex multiplier 54 for multiplying the I/Q data with the PN codes (PNLI, PNLQ) generated by the PN sequence generator;

a first low-pass filter 52 for smoothing an output of the first complex multiplier 51;

a second low-pass filter 55 for smoothing an output of the second complex multiplier 54;

a first amplitude detector 53 for detecting an output amplitude of the first low-pass filter;

a second amplitude detector 56 for detecting an output amplitude of the second low-pass filter;

a subtractor 57 for subtracting an output of the second amplitude detector 54 from an output of the first amplitude detector 53;

a loop filter 58 for smoothing an output of the subtractor 57; and

a voltage-controlled oscillator 59 fed with an output of the subtractor 57 as a control voltage; wherein

output clocks CK of the voltage-controlled oscillator 59 are routed to the PN sequence generator 60 and to the respective finger circuits (1, 6, 7, 8).

[0021]

In an embodiment of the present invention, each finger circuit includes a PN sequence generator 13 for generating the PN sequence (PNI, PNQ) subject to initial phase setting from a searcher, a complex multiplier 11 for multiplying the received input I/Q data with the PN sequence PNI, PNQ from the PN sequence generator 13 and a low-pass filter 12 for smoothing an output of the complex multiplier 11. An output of the low-pass filter 12 is output as a demodulated signal to the RAKE combiner 2.

[0022]

In an embodiment of the present invention, the phase of the PN sequence generator 60 in the DLL circuit 5 is aligned with the phase of the PN sequence generator 13 in the finger circuit as selected by the changeover circuit 4. In this case, the status (shift register value) of the PN sequence generator 13 in the as-selected one finger circuit is loaded on the shift register of the PN sequence generator 60 in the DLL circuit 5.

[0023]

In another preferred embodiment of the present invention, the PN sequence generator 13' in the finger circuit outputs PN codes (PNEI, PNEQ) earlier in timing than the PN codes used in the finger circuit (in-phase component PNI and quadrature component PNQ) and PN codes (PNLI, PNLQ) later in timing than the PN codes used in the finger circuit (in-phase component PNI and quadrature component PNQ). The PN sequences (PNEI, PNEQ, PNLI, PNLQ), output from the finger circuit as selected by the changeover circuit 4 are routed to the DLL circuit 5'.

[0024]

Referring to Fig.5, the DLL circuit 5' is fed with early PN codes (PNEI, PNEQ) and late PN codes (PNLI, PNLQ) as selected by the changeover circuit 4 and includes

a first complex multiplier 51 for multiplying received in-phase (I)/quadrature (Q) data with the early PN codes (PNEI, PNEQ), a second complex multiplier 54 for multiplying received in-phase (I)/quadrature (Q) data with the late PN codes (PNLI, PNLQ), a first low-pass filter 52

for smoothing an output of the first complex multiplier 51, a second low-pass filter 55 for smoothing an output of the first complex multiplier 55, a first amplitude detector 53 for detecting an output amplitude of the first low-pass filter 52, a second amplitude detector 56 for detecting an output amplitude of the second low-pass filter, a subtractor 57 for subtracting an output of the second amplitude detector 56 from an output of the first amplitude detector 53, a loop filter 58 for smoothing an output of the subtractor 57 and a voltage-controlled oscillator 60 fed with an output of the loop filter 58 as a control voltage. Output clocks of the voltage-controlled oscillator are routed to the respective finger circuits such that there is no necessity of providing a PN sequence generator in the DLL circuit 5'.

[0025]

[Preferred Embodiments]

For more detailed and specified description of the embodiment of the present invention, preferred embodiments of the present invention are explained with reference to the drawings, in which Fig.1 shows the structure of a RAKE receiver embodying the present invention. Data I (in-phase)/Q (quadrature) received following quasi-synchronization detection are fed to plural (n) finger circuits 1, 6, 7 and 8 where the phase adjustment is made from one multipath transmission path to another based on the path delay information as found by a searcher circuit, not shown.

[0026]

Demodulated signals from the finger circuits 1 and 6 to 8 (demodulated data) are fed to a RAKE combiner 2 so as to be synthesized

in the RAKE combiner 2 based on the path-based weighting algorithm for demodulation. The RAKE combiner 2 effects phase alignment of the outputs of the despreading correlators (finger circuits), while weighting the phase-aligned outputs in proportion to the signal level and summing the weighted outputs to enable maximal ratio combining of the powers of the respective paths to realize the path diversity effect. That is, the maximum ratio combining phase-aligns respective multipath branch signals (demodulated output signals of the respective finger circuits) to weight the respective branch signals in proportion to the signal level detected by the signal level detector to sum the resulting weighted branch signals. The higher the CN (carrier to noise) ratio and the larger the signal level of a given branch, the larger is the contribution of the branch to an output.

[0027]

Foe keeping the synchronization following initial acquisition, a DLL circuit 5 is used.

[0028]

In an embodiment of the present invention, a sole DLL circuit 5 is used to control the clocks CK of the entire finger circuits 1, 6 to 8 in the RAKE receiver, without providing one DLL circuit 5 for each of the finger circuits.

[0029]

If a RAKE receiver has e.g., m×n finger circuits, where m and n are preset positive numbers, it is of course possible to provide a common one DLL circuit in common for the n finger circuits and to provide a sum total

of m DLL circuits in the RAKE receiver, such that a plurality of units are provided, each of which comprised of one DLL circuit in common for a set of the finger circuits.

[0030]

The clocks CK are controlled based on the reception (in-phase)/Q (quadrature) data supplied to the DLL circuit 5 or on the path delay information as set in the finger circuits to be tracked, while the finger circuits used in controlling the DLL circuit 5 are selected by a changeover circuit 4.

[0031]

The switching of the changeover circuit 4 is controlled by a control circuit 3 fed with the finger-based weighting information as found by the RAKE combiner 2. The changeover circuit 4 includes a maximum value detection circuit, not shown, for detecting the maximum value of the weighting information input from the RAKE combiner 2 and which is afforded to the finger circuit. The control circuit 3 selects the finger circuit having the maximum weighting information and outputs a switching command signal to the changeover circuit 4 to switch to the selected finger circuit. Alternatively, the control circuit 3 may store the chronological data of the weighting information on the finger circuit basis as found by the RAKE combiner 2 in a memory, not shown, to analyze the chronological data to select the finger circuit which will give the maximum finger weighting information.

Fig.2 shows an illustrative structure of the DLL circuit 5 embodying the present invention. In Fig.2, the DLL circuit 5 is comprised of a

routine early-late gate circuit. The input I/Q data received is branched and is multiplied by a complex multiplier 51 by PN codes PNEI, PNEQ generated by a PN sequence generator 60. The PN codes PNEI, PNEQ are of timings earlier than the timing of the PN code used in a PN sequence generator of the finger circuit. In a complex multiplier 54, the received I/Q data is multiplied by the PN codes PNEI, PNEQ of the delayed frequency divider timing generated by the PN sequence generator 60.

[0033]

The PN sequence generator 60, generating and outputting PN codes, is comprised of a linear feedback shift register, made up of a shift register 601 and a parity generator (exclusive OR circuit) 602. The exclusive OR circuit 602 is fed with an output of one end (right end) of the shift register 601 and with an output of a preset stage (tap number) of the shift register 601, as inputs. An output signal of the exclusive OR circuit 602 is fed to an input at the other end (left end) of the shift register 601. In a well-known manner, the PN code generated by the PN sequence generator 60 has its characteristics determined by the length of the shift register 601, number or position of the tap input to the exclusive OR circuit 602 and by the initial value of the shift register 601. The early PN codes PNEI, PNEQ and the late PN codes PNLI, PNLQ are output from the positions on both sides of the take-out positions of the PN codes PNI, PNQ of the timings associated with the finger circuit.

[0034]

The outputs of the complex multipliers 51, 54 are synthesized by a

subtractor 57 through LPS (low-pass filters) 52, 55 and amplitude detectors 53, 56 and smoothed by a loop filter 58. The oscillation frequency of a voltage controlled oscillator (VC) 59 is variably controlled by an output signal of the loop filter 58 as a control signal. The VC 59 outputs clocks CK which are input as control clocks CK for the PN sequence generator 60. The clocks CK output by the VC 59 are fed not only to the finger circuit as selected, but also to the respective finger circuits.

[0035]

Fig.3 shows an illustrative structure of the finger circuits 1, 6, 7 and 8 in the embodiment of the present invention shown in Fig.1. Each finger circuit generates PN code strings PNI, PNQ, using a PN sequence generator 13 in which the initial phase setting is to be made from a searcher. The PN sequence generator 13 has the number of taps and the position for inputting to the parity generator in common (same) with those of a shift register of the same length as the PN sequence generator 60 of the DLL circuit 5.

[0036]

The input I/Q data, as received by th finger circuit, is multiplied in the complex multiplier 51 with the PN code strings PNI, PNQ, so as to be output through a low-pass filter (LBF.) 12 to the RAKE combiner 2.

[0037]

By the operation of the control circuit 3 and the changeover circuit 4, the DLL circuit 5 follows up with the phase jitter of one of the finger circuits 1, 6, 7 and 8, on which the maximum weight is put, based on the

synthesis algorithm of the RAKE combiner, to control the clocks CK supplied to the respective finger circuits.

[0039]

A variety of different configurations may be applied for aligning the phase of the PN sequence generator 60 in the DLL circuit 5 with the phase of the PN sequence generator 13 in the finger circuit to be tracked, as selected by the changeover circuit 4.

[0040]

In an embodiment of the present invention, the finger circuit to be tracked is selected by the changeover circuit 4, as shown in Fig.1, and the status of the shift register of the PN sequence generator in the selected finger circuit (shift register value) is loaded to the shift register 601 of the PN sequence generator 60 of the DLL circuit 5 through the changeover circuit 4 (see Fig.2).

[0041]

In an embodiment of the present invention, the register value of the shift register of the PN sequence generator 13 of each of the finger circuits 1, 6, 7, 8 (see Fig.3) is output to the changeover circuit 4. When the finger circuit is switched by the changeover circuit 4, the shift register value of the PN sequence generator 13 of the selected finger circuit is loaded on the shift register 601 of the DLL circuit 5.

[0042]

By the control circuit 3 sequentially controlling the changeover circuit 4, the DLL circuit 5 follows up with the phase of the finger circuit having a good signal state. On the other hand, the respective finger

circuits are phase-controlled by clocks CK output from the DLL circuit 5.

[0043]

A second embodiment of the present invention is now explained. Referring to Fig.4, showing the structure of the second embodiment of the present invention, the PN sequence generator of each of n finger circuits 1', 6', 7' and 8' outputs PN codes (PNEI, PNEQ, PNLI, PNLQ) at an early timing and a late timing to the changeover circuit 4, which then selects the early and late PN codes, output from the finger circuit selected by a switching command from the control circuit 3, to send the selected codes to a DLL circuit 5'.

[0044]

Fig.5 shows a structure of the DLL circuit 5' of the second embodiment of the present invention. Referring to Fig.5, the DLL circuit 5' of the second embodiment of the present invention is not in need of the PN sequence generator, in contradistinction from the DLL circuit 5 shown in Fig.2. In Fig.5, the PN code sequences (PNEI, PNEQ, PNLI, PNLQ) output from the finger circuit as selected by the changeover circuit 4 are supplied as the early and late PN codes input to the complex multipliers 51, 54.

[0045]

Output clocks of the VC 59 are routed to the respective finger circuits.

[0046]

Fig.6 shows the structure of the finger circuit in the second

embodiment of the present invention. In Fig.6, the finger circuit of the second embodiment of the present invention is basically of the same structure as the finger circuit of the previous embodiment shown in Fig.3. However, in the present second embodiment, the early and late PN code sequences (PNEI, PNEQ, PNLI, PNLQ) are output from the PN sequence generator 13' and routed through a signal line to the changeover circuit 4.

[0047]

That is, there is provided no PN sequence generator in the DLL circuit 5' so that the circuit scale can be reduced further as compared to that in the previous embodiment.

[0048]

Although the present invention has been explained in the foregoing with reference to preferred embodiments thereof, the present invention is not limited to these embodiments but may comprise various modifications which may come within the scope of the invention as defined in the claims.

[0049]

The meritorious effects of the present invention are summarized as follows.

According to the present invention, the operation of keeping synchronization is possible without the necessity of providing the DLL circuit in each finger circuit, so that meritorious effects may be achieved that the circuitry and hence the receiver may be reduced in size to achieve low power consumption.

It should be noted that other objects, features and aspects of the present invention will become apparent in the entire disclosure and that modifications may be done without departing the gist and scope of the present invention as disclosed herein and claimed as appended herewith.

Also it should be noted that any combination of the disclosed and/or claimed elements, matters and/or items may fall under the modifications aforementioned.